AMENDMENT TO THE SPECIFICATION

At page 1 at the first line following the title, please insert the following section:

REFERENCE TO RELATED APPLICATION

-- This is a division of Application No. 09/244,958, filed February 4, 1999, now issued as Patent No. (number not yet assigned).--

Kindly amend the specification as follows:

At page 12, following line 1, insert paragraphs [0001] through [0024].

[0001] The present invention provides a solution to the above problems by providing a process to control deposition of region 7 in a structure such as the transistor illustrated in Figs. 1 and 2. The processes and resulting structures may also be utilized in other applications. It just happens that the process of the invention is particularly useful in transistors such as those shown in Figs. 1 and 2.

[0002] By controlling the composition and physical characteristics of region 7, it follows that the present invention permits control of the value of beta in the resulting structure. The present invention accomplishes these and other objects by providing a process for creating a region of the material to form regions 7 in the structure illustrated in Figs. 1 and 2.

[0003] According to one embodiment, the present invention provides a rapid thermal oxidation (RTO) process. The rapid thermal oxidation process is utilized to form a layer of oxide on the surface of the emitter 5 illustrated in Figs. 1 and 2. The rapid thermal oxidation may be controlled to create oxide on at least of a portion of the emitter. In other words, it is not necessary that the oxide cover the entire emitter area. One factor that may control the thickness of the oxide as well as the percentage of the emitter covered by the oxide is the desired value of beta, which as stated above may be affected by the thickness of the oxide layer.

[0004] Among the variables that may be controlled in the rapid thermal oxidation process are temperature and time. According to one embodiment, the rapid thermal oxidation process is carried out at about 500°C. The rapid thermal oxidation process may be carried out for about 5 seconds. An embodiment of a process according to the present invention included rapid thermal oxidation carried out at about 500°C for about 5 seconds resulted in formation of an oxide layer having a thickness of about 6A. This oxide thickness includes about 4A of native oxide plus about 2A of oxide formed by the rapid thermal oxidation process. The resulting structure has a beta value of about 100. Without this process, the interface oxide was not well controlled and the resulting Beta value was at the low end of the process specification at a value of 60.

[0005] As referred to above, the silicon dioxide or oxide thickness described herein are defined as oxide that is thermally grown plus the native oxide already present on the wafer. For instance, after a preclean, a monocrystalline Si surface may include 5Å of native oxide as measured with an ellipsometer commonly used for semiconductor manufacturing. After subjecting this wafer to the rapid thermal oxidation process described herein, the oxide may measure 7A. In this case, the oxide thickness is defined as a thermally grown oxide of 2A in addition to or plus (+) native oxide of 5Å.

[0006] According to one example of the present invention, prior to deposition of the emitter polysilicon in bipolar transistor processing, the emitter monocrystalline silicon surface may be precleaned with some type of HF chemistry. Such chemistry is well know to those of ordinary skill in the art and, therefore, is not discussed further here. One of ordinary skill in the art could determine appropriate treatment including HF to utilize without undue experimentation.

[0007] All oxides may be removed from the surface of a monocrystalline silicon substrate such that only native oxide due to exposure of the silicon to the atmosphere remains on the silicon. At this time, typically, an oxide is grown on the surface of the monocrystalline silicon using a rapid thermal oxidation (RTO) process according to the present invention as described herein. The present invention typically results in the growth of about 1 A to about 5 A of thermal oxide. This level of thermal oxide is in addition to the native oxide present prior to the RTO process. The oxide level may be measured with an ellipsometer commonly used in semiconductor processing.

Therefore, if there is approximately 8A of native oxide prior to the RTO process, the measured thickness may be about 9 A to about 13 A post RTO. After the process of the present invention, polysilicon may then deposited in a CVD reaction without any additional oxidation of the Si surface.

[0008] Fig. 4 illustrates a relationship between the temperature at which the rapid thermal oxidation is carried out and the resultant thickness of the oxide layer between the emitter and the contact. As can be seen in Fig. 4, the total oxide as well as the oxide grown by the rapid thermal oxidation process both increase with increasing RTO temperature.

[0009] When polysilicon is deposited on the surface of the monocrystalline silicon substrate with different levels of thermally grown oxide as described above, the structures illustrated in Figs. 5-7 may result.

[0010] Fig. 5 shows a situation where polysilicon is deposited on a silicon surface with little oxide other than native oxide between the polysilicon and the monocrystalline silicon. The polysilicon seeds on the monocrystalline silicon base and the resulting polysilicon structure may include a significant level of epitaxially grown silicon containing many defects. In this case, the interfacial resistance is low and Beta will thus be low since the structure can result in high base current.

[0011] Where an interfacial oxide is present in range of less than about 5 A of thermally grown oxide plus native oxide, the structure illustrated in Fig. 6 results. In this case, the interfacial oxide **19** is not continuous. Where polysilicon is deposited over thin oxide, a normal polysilicon structure may result. Over the porous areas of the oxide film, the deposited silicon may be epitaxial silicon **17**. In this area, there is low resistance. Because the film is discontinuous but uniform, the interface typically is very good for controlling the base current and, thus, Beta. The extreme ideal for controlling the base current and thus Beta. Figure 6 depicts the interfacial oxide as a plurality of "islands" of oxide, **19**, separated by regions **17** of epitaxial silicon.

[0012] Fig. 7 illustrates an extreme case, where polysilicon is deposited on a monocrystalline silicon surface with a continuous oxide. The resulting film is entirely polysilicon with higher resistance than those described above. Thus, this structure results in high Beta.

[0013] A rapid thermal oxidation process according to the present invention may be carried out in a rapid thermal processor. Rapid thermal processors are devices that can heat substrates rapidly to a target temperature or temperatures, maintain the substrates at the target temperature(s), and cool the substrates rapidly from the target temperature(s). These devices are often used in semiconductor manufacturing where wafers are placed through thermal processes. A rapid thermal processor can heat wafers at rates of about 5° C to about 400° C/sec, with about 30° C/sec being typical. These processors can cool wafers at rates of about 5° C to about 100° C/sec, with about 30° C/sec being typical.

[0014] Typically, rapid thermal processors are single wafer processors. In other words, they do not process batches of substrates or wafers simultaneously. Instead, they process one wafer at a time through a prescribed thermal cycle. Because of this, the chamber of a rapid thermal processor typically is small, especially in comparison to the size of the chambers of used in conventional furnace hot processing.

[0015] Additionally, rapid thermal processing systems typically are closed systems, with control of gas delivery and exhaust. Therefore, during processing, gas concentrations may easily be controlled. For example, oxygen concentration may be controlled during processing at levels of from about 100% pure O2 down to about 10 ppm O2.

[0016] According to the process of the present invention, a layer of SiO_2 or other oxide layer may be formed over the monocrystalline semiconductor. The oxide layer may be described as a monolayer or less. Less than a monolayer indicates that not all of the surface of the monocrystalline semiconductor is covered with oxide. Less than a monolayer indicates the layer is discontinuous. Figure 3 illustrates the discontinuous layer of the present invention. Figure 3 depicts the oxide layer as comprising a plurality of isolated regions **19**. These isolated regions **19** may be termed "islands."

[0017] One significant advantage of the present invention is that it can produce a very repeatable oxide layer. In other words, the coverage and thickness of the oxide on the surface of the monocrystalline semiconductor are very repeatable according to the present invention.

[0018] As described above, the thickness of oxide created by the rapid thermal oxidation according to the present invention may vary depending upon the temperature, time, pressure, and/or oxygen concentration at which the rapid thermal oxidation is carried out. Increasing the temperature, time, pressure, or oxygen concentration will have the effect of increasing the thickness of oxide grown. Several different temperature ranges may be included in various embodiments of the present invention. For example, the invention may be carried out at a temperature less than about 700°C.

[0019] Selecting the target temperature of the rapid thermal process at least partially determines the thickness of the oxide layer grown. The specific electrical needs of a particular semiconductor device will determine what thickness of oxide is required. Depending upon the desired electrical characteristics of the devices being created, an extended range of temperatures may be used. Rapid thermal processes within the temperature ranges described herein can result in anywhere from complete coverage of the monocrystalline semiconductor to partial coverage of the monocrystalline semiconductor.

[0020] According to one embodiment of the present invention, a device may perform optimally with rapid thermal oxidation at a temperature of about 450° C. Another device may require a rapid thermal oxidation at a temperature of about 475° C. A typical range for rapid thermal oxidation processing according to the present invention is about 450° C to about 500° C. However, processing at less than about 450° C may result obtaining lower beta values. Processing above about 500° C may permit higher beta values to be obtained.

[0021] When temperatures in the vicinity of about 700° C are utilized, the resulting oxide layer may have a thickness of about 5Å to about 10Å. Alternatively though reductions in time, pressure, or oxygen concentration the oxide thickness may be no greater than about 5Å. Alternatively, the oxide layer may have a thickness of about 2Å to about 4Å or from about 2Å to

about 3Å when utilizing lower temperature processes. The specific thickness of oxide created may be determined by the rapid thermal oxidation process used, including manipulating the variables discussed herein.

[0022] As stated above, when a subsequent polycrystalline and/or amorphous semiconductor layer is deposited upon the semiconductor substrate, there is a tendency for the initial atoms of that added semiconductor layer to bond to the substrate with the monocrystalline pattern or orientation of the substrate. This is commonly referred to as epitaxial growth. The layer created by the present invention may provide a layer that reduces the tendency of that added semiconductor to deposit or grow epitaxially, or with the monocrystalline pattern of the substrate.

[0023] In the past, the problem of formation of single crystal semiconductor or monocrystalline semiconductor from polycrystalline and/or amorphous semiconductor was solved by oxidizing the surface of the monocrystalline semiconductor by bleeding O_2 gas or air in the polycrystalline semiconductor low-pressure chemical vapor deposition furnace. However, this method is known not to produce reliably repeatable results. Additionally, an O_2 or air bleed in a furnace does not permit all wafers to receive the same oxide monolayer or fractional oxide layer. Furthermore, the O_2 or air bleed typically results in a reduced number of fractional wafers in the furnace load. Also, in furnace processing with the air or O_2 bleed, processing each wafer to with its own specific process is not possible. In the single wafer rapid thermal oxidation process, each wafer or lot of wafers may receive a different rapid thermal oxidation process, if desired, allowing wafers to intentionally, and controllably reach a range of performance values.

[0024] Rather than an oxide layer, the layer between the monocrystalline semiconductor and polycrystalline and/or a amorphous semiconductor may be more broadly described as an electrically insulating material. The electric insulating material could be an oxide. However, it could also be a nitride and/or a nitridized oxide.

At page 11 delete the last two paragraphs, the material from page 11, line 6 through page 12, line 1; please insert the following material.

Fig. 3a illustrates an example of a structure that the present invention may be utilized with. Fig. 3a illustrates a region of monocrystalline silicon 1, a region of polycrystalline silicon 3 and an interface 5 between the region of monocrystalline silicon and polycrystalline silicon.

Fig. 3b illustrates a close-up cross sectional view of a portion of the structure illustrated in Fig. 3a including a plurality of regions of dielectric material between the two regions of semiconductor material. As such, Fig. 3b illustrates a portion of a structure showing an example of an embodiment of the structure according to the present invention. Along these lines, Fig. 3b illustrates a boundary region 7 including a plurality of regions 9 of dielectric material between the region of monocrystalline silicon 1 and the region of polycrystalline silicon 3. Arrows 12 represent current flowing between the regions of semiconductor material.